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EXAMINER
VIDWAN, JASJIT S

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2182	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS,
WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>19 May 2008</u>.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) <u>1,2,4-11,13-20,22-31 and 96</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) <u>1,2,4-11,13-20,22-31 and 96</u> is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All b) ☐ Some * c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage
          application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1.   Applicant's arguments, see Remarks, filed 05/19/08, with respect to independent claims have

been fully considered and are persuasive. The rejection of above claims has been withdrawn.

Claim Rejections - 35 USC § 103

1.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness

rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as
> set forth in section 102 of this title, if the differences between the subject matter sought to be
> patented and the prior art are such that the subject matter as a whole would have been obvious
> at the time the invention was made to a person having ordinary skill in the art to which said
> subject matter pertains. Patentability shall not be negatived by the manner in which the invention
> was made.

2.   Claims 1, 6-10, 15-19, 28-31 & 96 rejected under 35 U.S.C. 103(a) as being unpatentable over

Stancil, U.S. Patent No: 7,149,927 **[hereinafter Stancil]** and further in view of Luke et al, U.S. Patent No:

6,505,267 **[hereinafter Luke]** and Steely, Jr. et al, U.S. Patent No: 5,581,719 **[hereinafter Steely]**.

3.   **As per Claim 1, 10 & 19**, Stancil teaches an SMBus host controller **[Fig. 1, element 130]**

comprising:

        a.   SMBus interface **[see Fig. 1, element 111]**

        b.   SMBus message handler **[Fig. 1, element 110]** including finite-state machine **[Fig. 2,**

        elements 112 & 116] configured to manage data transfer between the SMBus interface and

        integrated electronic device **[Col. 4, Lines 20-32]**.

4.   Stancil further teaches a system wherein the said integrated electronic device's function is not

significant and thus can perform any functional logic **[see Col. 2, Line 66 – Col. 3, Line 2]**. Keeping the

scope of Stancil in mind, it is submitted that Stancil does not explicitly teach a memory storing microcode,

an interface to a register and further an instruction fetch unit configured to read instructions at an address

from said memory. Luke teaches the above deficiency in addressing the above deficiency by disclosing a system that teaches:

> (c) Memory **[See Fig. 2, element 32, 36 & 40]** configured to store microcode comprising at least two programs **[see Col. 7, Lines 58 – Col. 9, Line 12 – plurality of programs include 'Register read-modify-write', 'Register read-compare-until-match', 'Register Write', 'Register read extract nibble', 'Wait for bulk_in byte', Wait for bulk_out byte', 'DATI Push register into bulk_in', 'DATO Push bulk_out byte', 'EPPI Read EPP data register']** each for handling a bus command protocol and comprising at least one instruction **[see Col. 2, Lines 7-10 - - Also see Col. 4, Lines 66- Col. 5, Line 2]**.

> (d) Interface **[Col. 4, Lines 17-21]** to a register **[see Fig. 3, element 66]** configured to identify a starting address of a program in said memory **[Col. 4, Lines 34-37]**

> (e) Instruction fetch unit **[see Fig. 6, Element 90 – also see Col. 7, Lines 17-19]** configured to read an instruction at an address in said memory **[Col. 9, Lines 14-20]**, said address being specified by a program counter **[see Fig. 6, element 84]**

5.   It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the above two teachings in order to take advantage of using memory in conjunction with Stancil's SMBus Packet Decoder/Encoder **[see Fig. 2, element 114]** to support bus protocol conversion from host to the peripheral. It is for this reason that one of ordinary skill in the art would have been motivated to combine the above two teachings.

6.   Stancil and Luke teach the above limitations, however fail to teach an address register array comprising a plurality of starting addresses of programs stored in said memory. Steely teaches the above limitation of address register array comprising a plurality of starting addresses of programs stored in memory **[see Col. 3, Lines 22-45].**

7.   It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the above teachings in order to take advantage of retrieving instructions efficiently without devoting extensive resources to determine the starting addresses of programs **[see Col. 3, Lines 8-20]**. It

is for this reason that one of ordinary skill in the art at the time of Applicant's invention would have been

motivated to combine the above teachings.

8.   **As per Claims 6, 15 and 28,** Luke and Stancil as modified above teach SMBus message handler

further comprising a loop counter **[see Luke, Fig. 6, element 88]** for storing the value of a block counter

register in said loop counter if the finite-state machine executed a transmit data from block counter

register instruction **[see Luke, Col. 9, Lines 5-7, "DATO Push bulk_out byte into register"]**; said loop

counter being decremented each time a data byte is transmitted to said SMBus interface while a "transmit

data from" instruction is executed and the "transmit data from" instruction be completed when the value of

said loop counter reaches zero **[see Luke, Col. 7, Lines 43-51]**.

9.   **As per Claims 7, 16 and 29,** Luke and Stancil as modified above teach SMBus message handler

further comprising a loop counter **[see Luke, 88]** and a block counter register **[see Luke, 66]** both for

storing a byte received from said SMBus interface if the finite-state machine **[see Luke, 82]** executed a

"receive data to block counter register" instruction **[see Luke, Col. 9, Lines 8-11]**, said loop counter **[see

Luke, 204]** being decremented each time a data byte is transmitted to or received from said SMBus

interface while a "received data to block counter register " instruction is executed and the "received data

to" instruction being completed when the value of said loop counter reaches zero.

10.   **As per Claims 8, 17 and 30,** Luke and Stancil as modified above teach SMBus message

handler, wherein each instruction comprises one bit indicating as to whether or not an instruction is the

last instruction in the program **[see Luke, Col. 5, Lines 2-7]**.

11.   **As per Claims 9, 18 and 31,** Luke and Stancil as modified above teach SMBus message

handler, wherein each instruction comprises one bit indicating as to whether an instruction is to be

executed only once or this instruction is to be executed repeatedly until a loop counter becomes zero,

wherein said loop counter is decremented each time an instruction is executed repeatedly **[see Luke,

Col. 7, Lines 38-57]**.

12.   **As per Claim 96,** Luke and Stancil as modified above teach a controller wherein the memory

storing the microcode is a read-only memory **[see Luke, Fig. 2, element 36]**

13.   Claims 2, 4, 5, 11, 13, 14, 20, 22-27 rejected under 35 U.S.C. 103(a) as being unpatentable over

Stancil and Luke and further in view of Applicant Admitted Prior Art (Description of prior art) herein after

[AAPA].

14.   **As per Claims 2, 11 and 20**, Stancil and Luke teach the above limitations of claims 1, 10 and 19.

However, Luke fails to teach a system wherein the register set complies with the ACPI specification.

AAPA teaches the above deficiency of having a system wherein the register set is ACPI compliant **[see**

AAPA, Page 7, Paragraph 2 – Page 9, Paragraph 3].

           It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to

combine the teachings of Luke with that of AAPA in order to take advantage of a more efficient power

management interface with regards to the register set. It is for this reason that one of ordinary skill in the

art at the time of Applicant's invention would have been motivated to combine the teachings of Luke with

that of AAPA in order to take advantage of a more efficient power management interface with regards to

the register set.

15.   **As per Claim 4, 13 and 22**, Luke as modified by AAPA above teaches SMBus message handler

further comprising a buffer pointer register **[Fig. 6, element 92]** for pointing at one of a plurality of data

registers **[Fig. 3, element 66]**; said finite state machine **[Fig. 6, element 82]** transferring data read from

SMBus interface to the data register at which said buffer pointer register points if said finite-state machine

interprets a "receive data to" instruction; said finite state machine transferring the data read from the data

register at which said buffer pointer register points to **[Col. 7, Line 58-65]** said SMBus interface if said

finite-state machine interprets a "transmits data from" instruction **[Col. 8, Line 66-Col.9, Line 4]**

16.   **As per Claims 5, 14, 23 and 25** Luke as modified by AAPA above teaches SMBus message

handler wherein the finite-state machine causes said buffer pointer register to be incremented each time

a "transmit data to" or a "transmit data from" instruction is executed **[Col. 7, Lines 52-57]**

17.   **As per Claims 24 and 27,** Luke as modified by AAPA above teaches a method wherein said

transferring step further comprising decrementing a loop counter and checking as to whether said loop

counter has a value of zero **[Col. 8, Lines 3-13]**.

18.   **As per Claim 26,** Luke as modified by AAPA above teaches a method wherein said transferring

step further comprising incrementing of said buffer pointer register **[Col. 7, Lines 44-50]**

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should

be directed to JASJIT S. VIDWAN whose telephone number is (571)272-7936. The examiner can

normally be reached on 8am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tariq

Hafiz can be reached on 571.272.6729. The fax phone number for the organization where this

application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application

Information Retrieval (PAIR) system. Status information for published applications may be obtained from

either Private PAIR or Public PAIR. Status information for unpublished applications is available through

Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC)

at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative

or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-

1000.

/J. S. V./
Examiner, Art Unit 2182
8/17/08

/Tariq Hafiz/
Supervisory Patent Examiner, Art Unit 2182